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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/650,719	05/20/1996	JEFFREY S. MAILLOUX	95-0653	2941

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	44

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	08/650,719	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 16 October 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 6 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-9,33-35,46,48-50,59-61,63 and 64*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's argument on page 5 that improper rejection of claim 61 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification is not considered persuasive.

At page 5, applicant argues that the specification describes claimed limitation of "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", however, the examiner could not find support for this limitation. Also page 27 lines 5-11 only describes individual burst mode operation not while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation as claimed in the application.

Applicant's argument on page 7 that the reference does not disclose selecting between a burst mode and a pipeline modes of operations is not considered persuasive.

"The current invention include a pipelined architecture where memory access are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation, in other words, in order to work in a standard EDO memory including a pipeline architecture, one has to select pipeline mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. Therefore, given the teachings of above reference one of the ordinary skill in the art at the time the invention was made would have been lead to an obvious fashion to provide a pipelined EDO mode circuitry since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed.

Applicant's argument on page 8 that the reference does not disclose a mode circuitry, a buffer storing an address, a counter, and an EDO is not considered persuasive.

Manning discloses mode circuitry (col. 6 lines 14+), a buffer storing an address (Fig. 1 Ref. 18), a counter (Fig. 1 Ref. 26), and an EDO (col. 6 lines 21-22)..

HONG CHONG KIM
PRIMARY EXAMINER